GOVT. POLYTECHNIC NAYAGARH LESSON PLAN
session : 2023-2024

Discipline : ELECTRICAL ENGG.	Semester: 5th Sem	Name of the Teaching Faculty : Jadunath Murmu(Sr. Lect, in ETC)
Subject : DEC&MP	No. of Days / per week class allotted : 05	Semester From date : 1.08.2023 To Date : 30.11.2023
Week	**Class Day**	**Topics**
1st week August	1st	1. BASICS OF DIGITAL ELECTRONICS 1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	2nd	1.2 Binary addition, subtraction, Multiplication and Division.
	3rd	1.3 1's complement and 2's complement numbers for a binary number 1.4 Subtraction of binary numbers in 2's complement method.
	4th	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
2nd week August	1st	1.6 Importance of parity Bit. 1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	2nd	1.8 Realize AND, OR, NOT operations using NAND gates
	3rd	1.8 Realize AND, OR, NOT operations using NOR gates
	4th	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.
	5th	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression
3rd week August	1st	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression
	2nd	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
	3rd	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
	4th	Revision
4th week August	1st	Unit test
	2nd	2. COMBINATIONAL LOGIC CIRCUITS 2.1 Give the concept of combinational logic circuits. 2.2 Half adder circuit and verify its functionality using truth table
	3rd	2.3 Realize a Half-adder using NAND gates only and NOR gates only.
	4th	2.4 Full adder circuit and explain its operation with truth table.
	5th	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
5th week August	1st	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
	2nd	2.6 Full subtractor circuit and explain its operation with truth table.
	3rd	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
1st week Sept.	1st	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
2nd week Sept.	1st	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	2nd	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	3rd	2.9 Working of Two bit magnitude comparator.
	4th	2.9 Working of Two bit magnitude comparator.
3rd week Sept.	1st	REVISION
	2nd	Unit test
	3rd	3. SEQUENTIAL LOGIC CIRCUITS 3.1 Give the idea of Sequential logic circuits
	4th	3.2 State the necessity of clock and give the concept of level clocking and edge triggering
	5th	3.3 Clocked SR flip flop with preset and clear inputs.
4th week Sept.	1st	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	2nd	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	3rd	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.

4th week Sept.	1st	3.8 Applications of flip flops
	2nd	3.9 Define modulus of a counter 3.10 4-bit asynchronous counter and its timing diagram
	3rd	3.11 Asynchronous decade counter.
	4th	3.12 4-bit synchronous counter.
1st week October	1st	3.13 Distinguish between synchronous and asynchronous counters
	2nd	3.14 State the need for a Register and list the four types of registers.
	3rd	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
	4th	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
2nd week October	1st	REVISION
	2nd	4. 8085 MICROPROCESSOR 4.1 Introduction to Microprocessors, Microcomputers 4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	3rd	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	4th	4.3 Pin diagram and description.
	5th	**4.4 Stack, Stack pointer & stack top**
3rd week October	1st	4.5 Interrupts 4.6 Opcode & Operand, 4.7 Differentiate between one byte, two byte & three byte instruction with example.
	2nd	4.8 Instruction set of 8085 example
	3rd	4.9 Addressing mode 4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	4th	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	5th	4.12 Timing Diagram for 8085 instruction
PUJA HOLIDAY (21.10.2023 - 30.10.2023)		
1st week November	1st	4.13 Counter and time delay.
	2nd	4. 14 Simple assembly language programming of 8085.
	3rd	REVISION
2nd week November	1st	unit test
	2nd	5. INTERFACING AND SUPPORT CHIPS
	3rd	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	4th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 ,
	5th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 ,
3rd week November	1st	5.3 Application using 8255: Seven segment LED display,
	2nd	Square wave generator,
	3rd	Traffic light Controlle
	4th	REVISION
	5th	Unit test
4th week November	1st	REVISION
	2nd	REVISION
	3rd	REVISION
	4th	REVISION
	5th	REVISION
5th week November	1st	REVISION
	2nd	REVISION
	3rd	REVISION

Signature of Lecture/ Sr. Lect.

Signature of HOD